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The influence of the silicon nitride blocking layer thickness on the interface state densities (D_{it}) of HfO_2/SiN_x:H gate-stacks on n-type silicon have been analyzed. The blocking layer consisted of 3 to 7 nm thick silicon nitride films directly grown on the silicon substrates by electron-cyclotron-resonance assisted chemical-vapor-deposition. Afterwards, 12 nm thick hafnium oxide films were deposited by high-pressure reactive sputtering. Interface state densities were determined by deep-level transient spectroscopy (DLTS) and by the high and low frequency capacitance-voltage (HLCV) method. The HLCV measurements provide interface trap densities in the range of 10^{11} cm^{-2} eV^{-1} for all the samples. However, a significant increase in about two orders of magnitude was obtained by DLTS for the thinnest silicon nitride barrier layers. In this work we probe that this increase is an artifact due to the effect of traps located at the internal interface existing between the HfO_2 and SiN_x:H films. Because charge trapping and discharging are tunneling assisted, these traps are more easily charged or discharged as lower the distance from this interface to the substrate, that is, as thinner the SiN_x:H blocking layer. The trapping/detrapping mechanisms increase the amplitude of the capacitance transient and, in consequence, the DLTS signal that have contributions not only from the insulator/substrate interface states but also from the HfO_2/SiN_x:H interlayer traps. © *2010 American Institute of Physics*. [doi:10.1063/1.3391181]

I. INTRODUCTION

The scaling down of metal-oxide-semiconductor field effect transistors has allowed the integration of a large number of transistors in a chip. However, as the effect gate oxide scales toward 1 nm, the resulting leakage gate current due to direct tunneling rises unacceptably. An alternative gate dielectric should be shortly introduced to replace SiO_2, but this task is not trivial. In order to achieve performances comparable to those of silicon oxide, high-k dielectrics have to fulfill some requirements apart from its high permittivity: high band gap and barrier offsets relative to silicon, thermodynamic stability, high quality interface, low density of defects, reliability, and compatibility with the actual complementary metal-oxide-semiconductor technology.[1–3]

HfO_2 is among the most promising high-k dielectrics, but before qualifying, the nature and formation of electrically active defects existing in these emerging materials should be known. In fact, hafnium based high-k dielectric are already in production. In early 2007, Intel announced the deployment of hafnium based high-k dielectrics in conjunction with a metallic gate for components built on 45 nanometer technologies, and has shipped it in the 2007 Penryn microprocessor series.[4,5] In 2008, IBM announces the alliance of several foundries to fabricate 32 nanometers technology in the basis of a "High-k/Metal Gate" material.[6] While not identified, it is most likely the dielectrics used by these companies are some form of nitrided hafnium silicates (HfSiON). HfO_2 and HfSiO are susceptible to crystallization during dopant activation annealing. However, even HfSiON is susceptible to trap-related leakage currents, which tend to increase with stress over device lifetime. This drawback increases with the hafnium concentration. It is known that defects in SiO_2 are passivated by hydrogen, but this can cause some problems in HfO_2.[7] Moreover, HfO_2, as most of the high-k materials, when deposited in direct contact with Si an interfacial layer (few nanometers thick) is formed.[8] We have confirmed, in an earlier work, the formation of silicon oxide (SiO_x) as interfacial layer when depositing HfO_2 directly on Si.[9] Because of the noncontrolled nature of the silicon dioxide layer, the interfacial state density (D_{it}) and leakage current can increase. Moreover, this barrier layer leads to a reduction in the dielectric constant and, hence, to the effective capacitance of the gate dielectric stack. The use of silicon nitride instead of silicon oxide as barrier layer can improve the effective capacitance of the gate dielectric stack, since silicon nitride has a higher permittivity ($\approx$7) than silicon oxide ($\approx$3.9). Moreover, SiN_x is stable when deposited on Si, preventing the growth of silicon oxides, and the use of nitrides greatly reduces boron diffusion from the heavily doped poly-Si gate electrode to the lightly doped Si channel.[10]

In this work, we focus our attention on the interface density measured by two techniques: deep-level transient spectroscopy (DLTS) and simultaneous high and low frequency capacitance-voltage (HLCV). Specifically, we have compared the results of these two techniques when applied to

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TABLE I. Electron-cyclotron-resonance assisted chemical-vapor-deposition (ECR-CVD) deposition time, silicon nitride thickness, and interface state densities provided by DLTS and HLCV measurements.

Sample	ECR-CVD time (s)	Silicon nitride thickness (nm)	RTA	D_{it} from DLTS $\times 10^{11}$ ($cm^{-2}\,eV^{-1}$)	D_{it} from HLCV $\times 10^{11}$ ($cm^{-2}\,eV^{-1}$)
Asd_1	90	6.6 ± 0.4	As-deposited	3–5	3.0
RTA_1			600 °C–30 s	2–5	2.2
Asd_2	60	5.9 ± 0.4	As-deposited	0.8–1	1.3
RTA_2			600 °C–30 s	1–2	2.7
Asd_3	30	3.9 ± 0.2	As-deposited	Not measured	4.5
RTA_3			600 °C–30 s	100–200	4.4
Asd_4	15	3.0 ± 0.4	As-deposited	50–100	2.0
RTA_4			600 °C–30 s	50–100	1.9

$Al/HfO_2/SiN_x:H/n\text{-}Si$ capacitors and we have studied the effect of $SiN_x:H$ thickness, t_{bl}, in the D_{it} measurement while keeping constant the thickness, t_{hk}, of the high-k (HfO_2) dielectric film. Since t_{hk} does not change, the high-k dielectric must show the same properties for all the samples and we cannot attribute the discrepancies to any mechanism occurring in it. On the contrary, as t_{bl} diminishes, tunneling from the silicon substrate becomes important and states localized at the interface between the two dielectric films can more easily interchange carriers with the silicon substrate.

II. EXPERIMENTAL

Metal-insulator-semiconductor (MIS) structures were obtained as follows: substrates were 500 μm thick wafers (polished on one side) of 5 Ω cm n-type silicon. Before the dielectric growing, the substrates were submitted to a standard Radio Corporation of America cleaning. Deposition of silicon nitride was conducted in a home-made chamber attached to an electron-cyclotron-resonance (ECR) Astex 4500 Reactor. A mixture of high purity silane (SiH_4) and N_2 were used as precursors. Deposition times were 90, 60, 30, and 15 s giving rise to four different thicknesses (6.6 nm, 5.8 nm, 3.9 nm, and 3 nm, respectively). Two series were obtained for each thickness, being one of them submitted to a rapid thermal annealing (RTA) at 600 °C for 30 s. Afterwards, 12 nm HfO_2 films were grown in a high-pressure sputtering system[11] at pressure of 1.2 mbar during 30 min, keeping the temperature at 200 °C. High-k dielectric films were grown in a pure Ar atmosphere, because, as shown on a preliminary study,[12] these films present an amorphous structure. After the dielectric deposition, aluminum dot electrodes were e-beam evaporated through a shadow mask. Table I lists the samples obtained and the DLTS and HLCV experimental results.

Electrical measurements were carried out by putting the sample in a light-tight, electrically shielded box. In order to record electrical parameters at temperatures varying between room temperature and 77 K, samples were cooled in an Oxford DM1710 cryostat. An Oxford ITC 503 temperature controller was used to measure and control the measuring temperature. C-V setup consists of 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. To determine the interface trap densities we used DLTS and HLCV techniques in order to contrast the results obtained by the two techniques. As is well known, HLCV consist on comparing high frequency (1 MHz) and quasistatic C-V measurements. For the quasistatic measurement, we record the gate current whereas a ramp-voltage is applied to the gate terminal. A Keithley 82 system is used to this technique. DLTS measurements consisted on recording and processing 1 MHz isothermal capacitance transients at temperatures from 77 K to room temperature. A Keithley 617 programmable electrometer is used together with an HP214B pulse generator to introduce the quiescent bias and the filling pulse, respectively. D_{it} is obtained by applying a pulse that drives the MIS capacitor to accumulation, in order to fill the interfacial traps. Afterwards the bias quickly returns to the limit between depletion and weak inversion, then traps formerly filled are emptied yielding the capacitance transients, which are recorded for the DLTS processing. The isothermal capacitance transients are captured by a 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope. The digital oscilloscope allows us to record the entire capacitance transient and, in this way, we can process the entire energy spectrum with only one temperature scan.

III. RESULTS AND DISCUSSION

A. Experimental data analysis

HLCV measurements are summarized in Table I. This technique provides similar interface density (D_{it}) values ($2-4\times 10^{11}$ $cm^{-2}\,eV^{-1}$) for all the samples, regardless the silicon nitride layer thickness. Therefore, interface quality seems not to depend on the blocking layer thickness, as one could expect for these not extremely thin films. In contrast, DLTS results (Fig. 1) can be clearly separated in two groups: one corresponding to the thickest samples which have D_{it} densities from 9×10^{10} to 4×10^{11} $cm^{-2}\,eV^{-1}$, in good agreement with HLCV results. The second group corresponds to the thinnest samples with D_{it} values (from 6×10^{12} to 2×10^{13} $cm^{-2}\,eV^{-1}$) much higher than those obtained by HLCV. In order to explain these discrepancies we have carried out an exhaustive analysis that leads us to conclude that charging and discharging mechanisms of inner traps existing at the HfO_2/SiN_x interface affect the DLTS results.

Figure 2 plots the normalized C-V curves measured at room temperature for the as-deposited samples. The stretch-out observed is similar in all the samples, meaning a similar trap density, contrary to the DLTS results. Vuillame *et al.*[13]

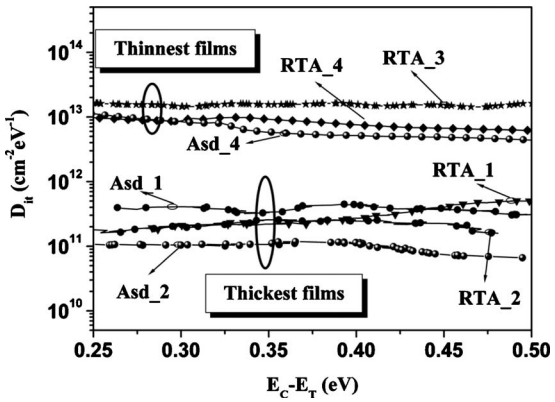

FIG. 1. Interface state density measured by DLTS.

observed variations in the DLTS signal due to slow traps located inside the insulator, but these changes are only observed for very short filling accumulation pulses times under 50 μs, much lower than the 15 ms used in our experiments. On the other hand, changes were much smaller than those observed in this work. Moreover, slow traps induce hysteresis at the C-V curves and conductance transients. However, a clockwise hysteresis is observed only in the thickest samples and conductance transients have not been detected in any of the thinnest samples. The only difference between the samples is the HfO_2/SiN_x:H interface distance from the substrate, so that we focused our attention in the traps existing at the surface between the SiN_x:H interface layer and the HfO_2 film.

To study these discrepancies in depth, we have focused our attention on the sample showing the biggest discrepancies on the D_{it} values measured by HLCV and DLTS. The one selected has been the Asd_4 sample, which has the lowest barrier layer thickness (3 nm). In order to determine the electric filed influences, we have recorded the interface state density profiles obtained by DLTS when varying the bias conditions. Figure 3(a) shows important variations in the D_{it} profiles when the accumulation filling pulse voltage is varied while keeping constant the reverse voltage. On the contrary, no significant differences are obtained when varying the reverse voltage [Fig. 3(b)]. Therefore, the mechanisms responsible for these variations must occur during the trap-filling pulse but not under reverse (detrapping) bias conditions, when the capacitance transients are recorded.

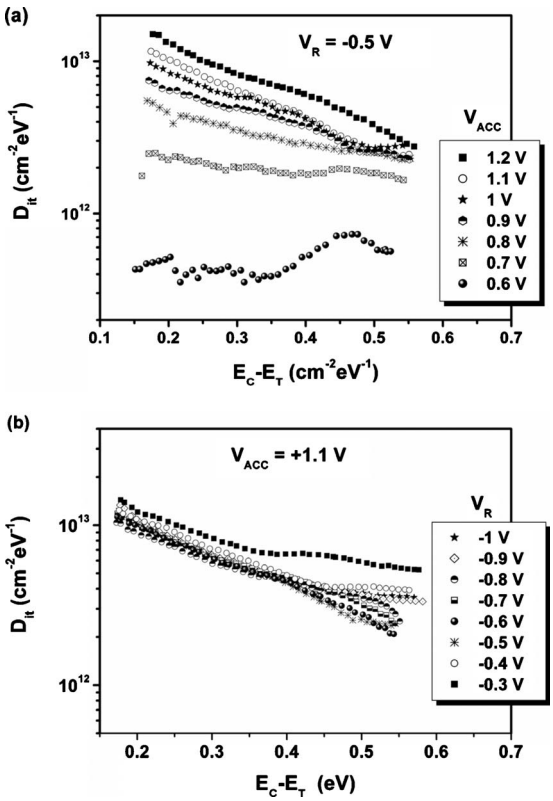

FIG. 3. (a) DLTS profiles obtained keeping constant the voltage of the reverse-emptying-pulse and (b) the accumulation filling pulse.

In Fig. 4, we show the DLTS values obtained for different energies as a function of gate voltage and the electric field at the silicon nitride film. The electric field has been evaluated according the expression

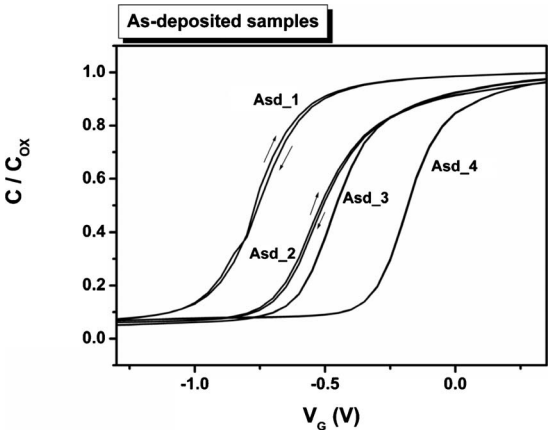

FIG. 2. 1 MHz C-V curves measured for the as-deposited samples at room temperature.

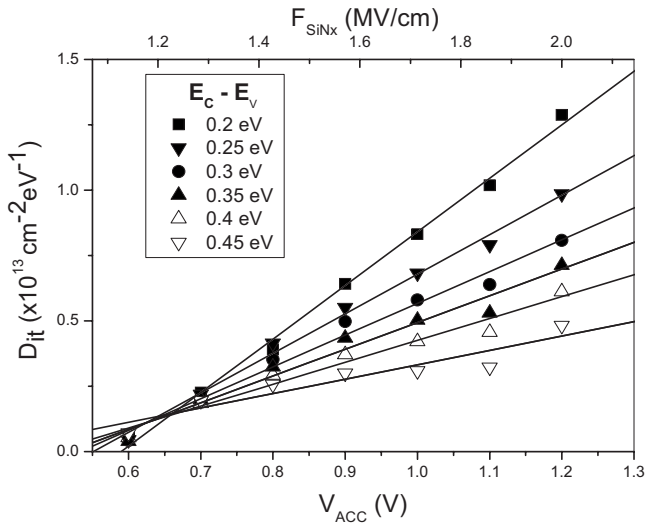

FIG. 4. Experimental DLTS signal as a function of accumulation voltage and SiN_x electric field for different energies.

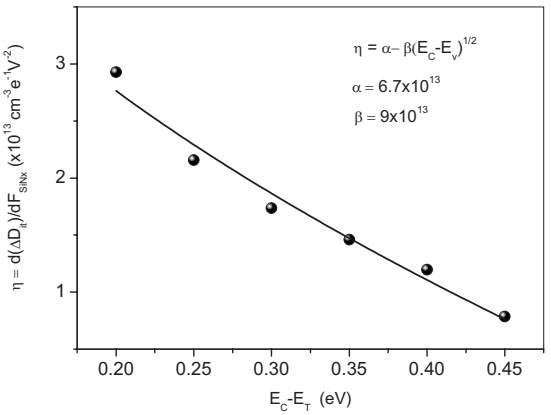

FIG. 5. Variation with energy of the electric field barrier lowering parameter, η.

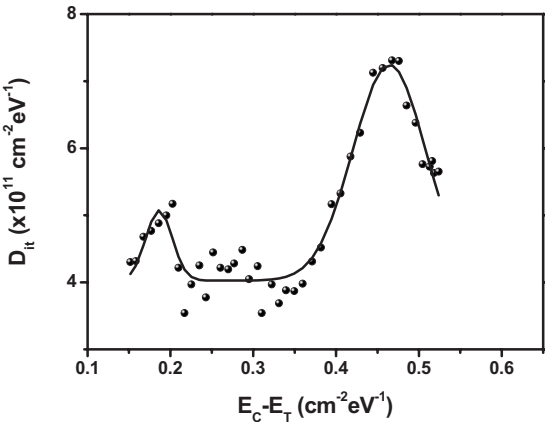

FIG. 6. True interface state density profile as obtained at low electric fields (<1 MV cm^{-1})

$$F_{\mathrm{SiN_x}} = \frac{V_G - V_{FB}}{\frac{\varepsilon_{\mathrm{SiN_x}}}{\varepsilon_{\mathrm{HfO_2}}} t_{\mathrm{HfO_2}} + t_{\mathrm{SiN_x}}}. \quad (1)$$

We clearly observed that for all the energies the relationship between D_{it} and electric field is linear

$$\frac{d\mathrm{D_{it}}}{dF_{\mathrm{SiN_x}}} = \eta(E_c - E_T). \quad (2)$$

The slope of Eq. (2) is a function of energy. This dependency is plotted in Fig. 5 and we have observed that the experimental points fit very well the following dependency:

$$\eta(E_c - E_T) = \alpha - \beta\sqrt{E_C - E_T}. \quad (3)$$

In summary, we can state that experimental DLTS profiles obey the following expression:

$$\mathrm{D_{it}^*} = \mathrm{D_{it}} + \eta F_{\mathrm{SiN_x}} = \mathrm{D_{it}} + (\alpha - \beta\sqrt{E_c - E_T})F_{\mathrm{SiN_x}}, \quad (4)$$

where D_{it}^* is the as-measured apparent interface state profile. D_{it} is the true trap interface state density profile that is the obtained at low electric filed values. η is a parameter associated to the electric field lowering of the energy barrier between the silicon conduction band and traps located at the inner layer interface (IL). This barrier is lower as higher the energy of the inner interface layer traps and this fact is included at the term $\beta\sqrt{E_c - E_T}$.

The true interface state density, D_{it}, is plotted at Fig. 6 as obtained for the lowest accumulation voltage values. These values do agree with those obtained when using HLCV technique. Moreover, this distribution show a profile consisting on broad Gaussian peaks, as is usually reported for silicon nitride films.[14–18]

B. Band energy model

The energy diagrams of the MIS structures under accumulation and inversion are displayed in Fig. 7. To construct them, we have included the published values of the band gap and the conduction and valence band offsets of hafnium oxide and silicon nitride relative to silicon.[19] We also assume that defects exist at the HfO_2/SiN_x:H IL. DLTS measurements consist of applying accumulation pulses to fill the interface states in the upper half of the semiconductor band gap followed by reverse pulses in which the interface states emit electrons to the conduction band yielding the capacitance transients that are conveniently recorded and processed to obtain the D_{it} distribution. If the SiN_x:H film is thin enough, tunneling between the semiconductor and the IL may occur. At accumulation, capturing electrons coming from the semiconductor band by direct tunneling fills IL states. Then, when the reverse pulse is applied, these defects emit the captured electrons to the semiconductor band. The emission process may occur in two different ways: IL states with energies above the silicon conduction band (light gray area) emit elec-

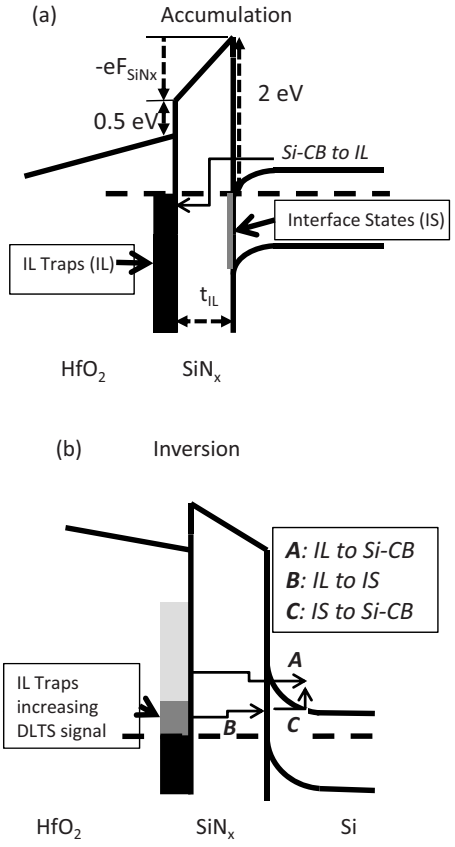

FIG. 7. Energy band diagrams of the HfO_2/SiN_x:H/n-Si MIS structures under (a) accumulation and (b) inversion.

trons by direct tunneling (A). On the other hand, for energies ranging from the Fermi level to the semiconductor conduction band (dark gray area) tunneling between the IL states and the interface states (B). These interface states can emit electrons to the conduction band in a similar way as occurs in conventional DLTS (C). Electrons emitted according the (B)+(C) sequence increase the capacitance transient, obtaining an apparent increase in the measured interfacial state densities. Since all these mechanisms are tunneling assisted, as thinner the silicon nitride films as higher their probability. In our experiment, the SiN_x:H layer thickness has been varied from around 3 to 6.6 nm. To roughly estimate the relationship between the tunneling charging/discharging probabilities for two samples with different silicon nitride thickness (t_1 and t_2), we can use the following quantum mechanics expression:

$$\frac{p_1}{p_2} = \exp\left[\frac{2\pi\sqrt{2m_h\overline{\varphi_V}}}{h}(t_1 - t_2)\right], \tag{5}$$

where m_h is the hole effective mass inside the barrier, $\overline{\varphi_v}$ is the mean barrier height, t_1 and t_2 are the barrier thickness, and h is the Plank's constant. For the h-well triangular barrier, $\overline{\varphi_v}=\Delta E_V/2$, where ΔE_V is the valence band offset of silicon nitride relative to silicon. Gritsenko and Meerson[20] reported values of $\Delta E_V \approx 1.5$ eV and $m_h/m_0=(0.3\pm0.1)$. Here m_0 is the free electron mass. These values yield a relation of $p_1/p_2=10^{-4}$ for two layers of 6 nm and 3 nm, respectively, so indicating that the IL trapping/detrapping mechanisms effect is negligible for thicker samples in comparison with the 3 nm thick blocking layer samples where the very thin silicon nitride layer allows electron tunneling from IL traps to the channel interface, so increasing the total charge emitted during the DLTS reverse pulses.

Moreover, an increase in the filling electric field in Fig. 7(a) (higher bias in the accumulation regime) causes a larger number of IL filled traps. Then, when biasing the sample in the inversion regime, a higher number of IL traps can contribute to the capacitance transient by direct tunneling. This result agrees with results shown in Fig. 3(a): the higher the filling pulse the higher the DLTS D_{it} results.

On the contrary, variations in the inversion bias do not change the total filled traps, and the emitted charge from the IL traps does not change significantly. The results shown in Fig. 3(b) confirm this hypothesis: the measured D_{it} values hardly change when varying the reverse bias.

In samples with thicker SiN_x:H layer, IL traps cannot contribute to the DLTS capacitance transients, which take place in a relatively short time. However, the IL traps in these samples do exchange charge with the substrate in longer times, giving rise to the hysteresis phenomena not observed in the two thinnest samples. In fact, we can measure slow states inside the MIS insulator by the conductance transient technique (GTT).[21] We have measured the slow states inside the insulator and we have observed only slow states in the two thickest samples: if these slow states were due to traps in the bulk SiN_x:H, they would appear in all the samples.

IV. CONCLUSIONS

The significant increase on the interface density of about two orders obtained by DLTS for very thin silicon nitride layers in HfO_2/SiN_x:H gate stacks is an artifact caused by tunneling assisted charging and discharging of traps existing at the HfO_2/SiN_x:H interlayer interface. The trapping/detrapping mechanisms increase the capacitance transient and, in consequence, the DLTS measurements have contributions not only from the insulator/substrate interface but also from the HfO_2/SiN_x:H interlayer interface. As the DLTS filling pulse increase, the D_{it} obtained move away from the expected value. The measurement of the slow states inside the insulator by GTT confirms this hypothesis. In summary, we can conclude that interface state densities obtained by DLTS in the specific case of the HfO_2/SiN_x:H/Si system provides overestimated D_{it} values for very thin silicon nitride layers. A detailed analysis of the experimental data allowed us to derive the physical and mathematical model for this anomalous behavior.

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